Electronic Properties of Stacked ZrO_2 Films Fabricated by Atomic Layer Deposition on 4H-SiC

Krystian Król [1], Norbert Kwietniewski [1], Sylwia Gierałtwoska[2], Łukasz Wachnicki[2], Mariusz Sochacki[1]

[1] *Institute of Microelectronics and Optoelectronics, Warsaw University of Technology, Koszykowa 75, 00-662 Warsaw, Poland*
[2] *Institute of Physics Polish Academy of Science, al. Lotników 32/46, 02-688 Warsaw, Poland*

It is shown that optimum electronic devices based on wide bandgap semiconductors such as silicon carbide provide the basis for wide field of applications including power conversion at relatively high frequencies. Silicon carbide based MOSFET can be used in high current applications working with high electric fields. In recent years a number of studies have been published for investigation of SiO_2/SiC interface aimed for gate dielectric for MOSFETs. Since the effective electric field in silicon carbide devices is generally to strong for the most widely used silicon dioxide it is a new trend of investigation to develop high-k dielectric materials that can overcome this problem. The use of silicon dioxide as a gate dielectric film is far from optimal capabilities of silicon carbide devices. Silicon carbide has large critical electrical field of ~3 MV/cm, much larger than commonly used silicon (Si) at relatively high permittivity of 9.66. On the other hand it has been shown that silicon dioxide long-term stability is assured for fields lower than ~2 MV/cm. Gauss law for classical SiO_2/4H-SiC interface indicates that electrical breakdown or long-term degradation is expected in SiO_2 layers for electric fields much lower than expected in silicon carbide substrate. Thus in SiO_2/4H-SiC interface the superior properties of SiC cannot be exploited. The implementation of high-k dielectric films in silicon carbide technology is still under investigation mainly due to low band offset between commonly used dielectric materials and silicon carbide.

In this work we report the electrical properties of zirconium oxide/silicon dioxide (ZrO_2/SiO_2) stacked layers applicable for use in SiC MOSFET technology. A ZrO_2 layers were fabricated within temperature range of 85-250°C using atomic layer deposition technique on 4H-SiC(0001) substrates covered by thin (~10 nm) layer of thermal SiO_2. MOS structures were manufactured using these stacked layers as gate dielectric. These structures were subjected to series of electrical testing utilizing IV and CV measurements and a comprehensive electronical characterization was performed. Electrical properties of stacked ZrO_2/SiO_2 layer depends strongly on temperature of ALD process resulting in wide range of permittivity (k = 16-25) for the process temperature of 85-250°C. As the permittivity of the layer increases the electric field in the SiO_2 thin layer also increases changing the conduction mechanism in gate dielectric and applicable voltage range. It has been shown that very large values of electrical permittivity are not beneficial for discussed application. The properties of the stacked dielectric films are then dominated by silicon dioxide buffer layer under high electric field. . It leads to a reduction of breakdown voltage. However, increased performance of MOS structures with moderate electric permittivity values of high-k dielectric films was confirmed clearly in this work.

ACKNOWLEDGEMENTS
The presented results are an output of project “Oxide nanostructures for electronics, optoelectronics and photovoltaics” funded by National Science Centre (UMO-2012/06/A/ST7/00398).