# An influence of silicon substrate parameters on a responsivity of MOSFET-based THz detectors.

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Silicon field effect n-type MOSFETs have been recently used as terahertz (THz) radiation detectors. They are cheap, easy to integrate with silicon read-out and offer reasonable detectivity at room temperature. Their response, i.e. a DC voltage measured between the source and unbiased drain is proportional to a power of an incoming radiation. The response maximum is typically achieved at subthreshold range. The MOSFETs may be easily equipped with patch antennas fabricated on top of the circuit. It has been shown that an effective imaging with use of FETs can be achieved in atmospheric windows of 300 GHz and 600 GHz.

The effective coupling of the FET channel with the THz wave is strongly influenced by the fact that part of radiation is dissipated within the substrate. That may be minimized by thinning the substrate using a grinding technique or by fabricating the detectors on membranes using MEMS-related technologies. Highly resistive substrates may be also used especially if the detector backsides are exposed to radiation via dedicated glued lenses machined using highly resistive silicon. In this paper we examine several types of different substrates to make a suitable choice for a volume production of NMOSFET-based THz detectors.

The NMOSFETs with polysilicon gate and monolithically coupled antennas and with projected channel length of 3 μm have been used. They have been manufactured on the following substrate types: Silicon-On-Insulator (SOI) wafers, low resistivity Czochralski (Cz-Si) wafers, and high resistivity (HR) floating zone (FZ) wafers.

The substrates of the devices have been thinned down to 40 μm. In the case of SOI and Cz-Si wafers the membranes have been manufactured using a selective etching, while in the case of HR FZ wafers the grinding technique has been initially used. The selective etching in KOH solution could not have been applied in this case because of the wafer orientation (111). However, recently the detectors on (100) HR FZ wafers with membranes have been also processed.

The measurements of the MOSFET responsivity (DC voltage between drain and source) have been done. The largest response (100 μV) has been measured for MOSFETs on the SOI wafers with the local membranes. The response of 10÷20 μV has been achieved for MOSFETs on the thinned HR FZ wafers. The response of 1÷2 μV has been achieved for devices on membranes on the Cz-Si wafers. The recent measurements have revealed a high responsivity of the MOSFETs on membranes manufactured on HR FZ wafers, in some cases even higher (~500 μV) than for SOI wafers. This result is interesting not only from a research point of view, but also from manufacturing aspect - among others the HR FZ wafers are significantly cheaper than the SOI substrates. So the fabrication of the THz detectors on the HR FZ wafers becomes a promising option with respect to SOI-based technology.

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